CYPRESS SEMICONDUCTOR

CY6116

2048 x 8 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed—35 ns**
- **Low active power — 660 mW**
- **Low standby power — 110 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

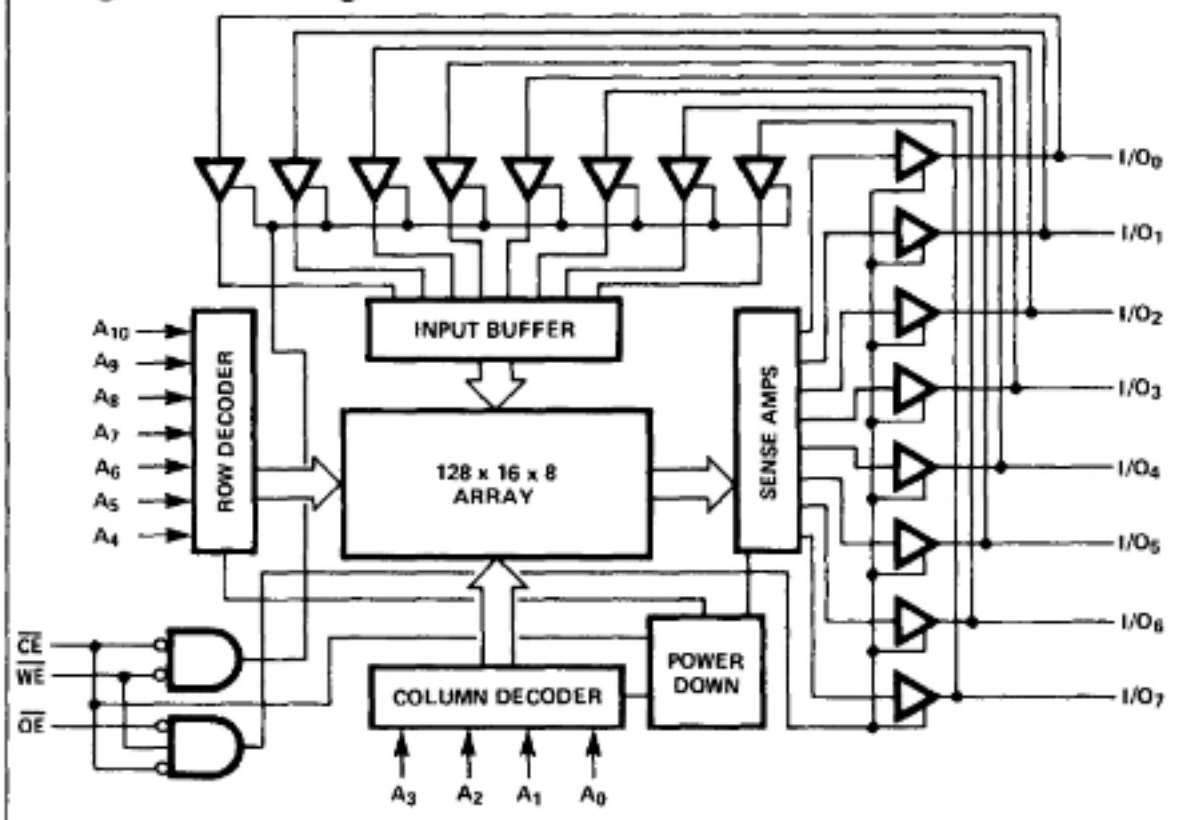
The CY6116 is a high performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), and active LOW output enable ($\overline{OE}$) and three-state drivers. The CY6116 has an automatic power-down feature, reducing the power consumption by 83% when deselected.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{10}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

The CY6116 utilizes a die coat to ensure alpha immunity.

Logic Block Diagram



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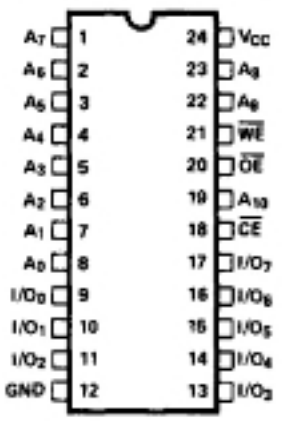
Pin Configurations



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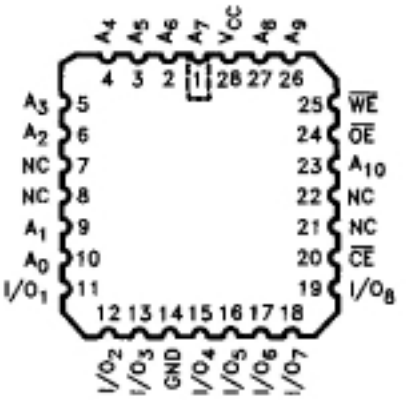

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Selection Guide

		CY6116-35	CY6116-45	CY6116-55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commercial	120	120	120
	Military	130	130	130
Maximum Standby Current (mA)	Commercial	20	20	20
	Military	20	20	20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015)

Latch-up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[4]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range[3]

Parameters	Description	Test Conditions		CY6116-35, 45, 55 Min.	CY6116-35, 45, 55 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC} Output Disabled			10	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		120	mA
			Military		130	
I_{SB}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Commercial		20	mA
			Military		20	

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested initially and after any design or process changes that may affect these parameters.
3. See the last page of this specification for Group A subgroup testing information.
4. T_A is the "instant on" case temperature.

AC Test Loads and Waveforms

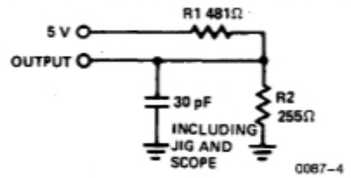


Figure 1a

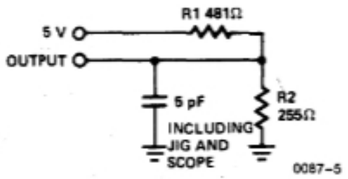


Figure 1b

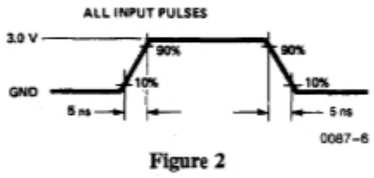
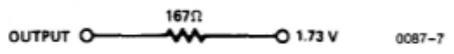


Figure 2

Equivalent to:

THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range[4, 6]

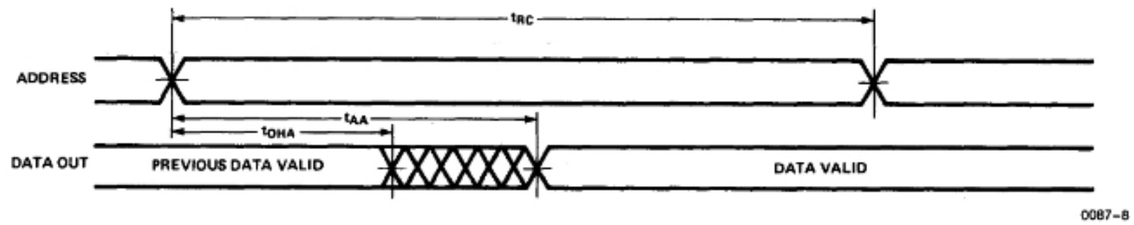
Parameters	Description	6116-35 Min.	6116-35 Max.	6116-45 Min.	6116-45 Max.	6116-55 Min.	6116-55 Max.	Units
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		15		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		15		20		20	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		20		25		25	ns
WRITE CYCLE[9]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	30		40		40		ns
t_{AW}	Address Set-up to Write End	30		40		40		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	WE Pulse Width	20		20		25		ns
t_{SD}	Data Set-up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z		15		15		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns

Notes:

5. Data I/O Pins enter high-impedance state, as shown, when $\overline{OE}$ is held LOW during write.
6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
7. t_{HZOE}, t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in *Figure 1b*. Transition is measured ± 500 mV from steady state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

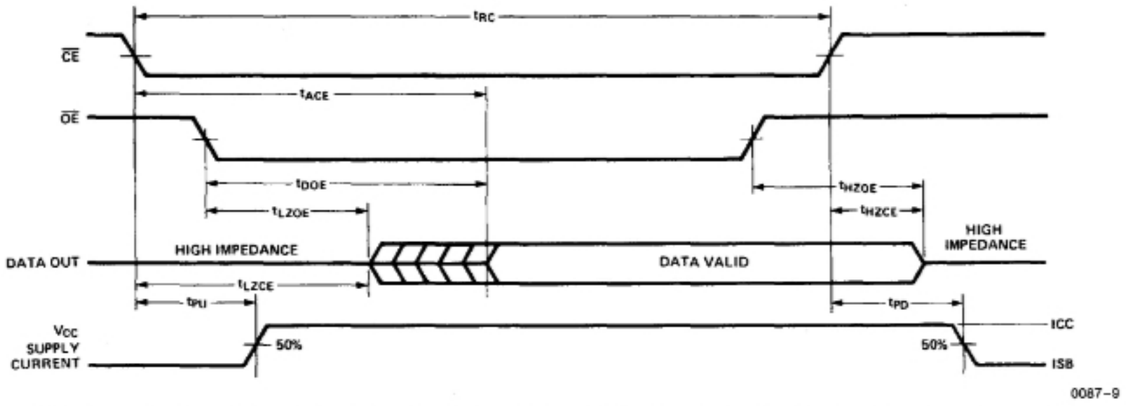
Switching Waveforms

Read Cycle No. 1 (Notes 10, 11)

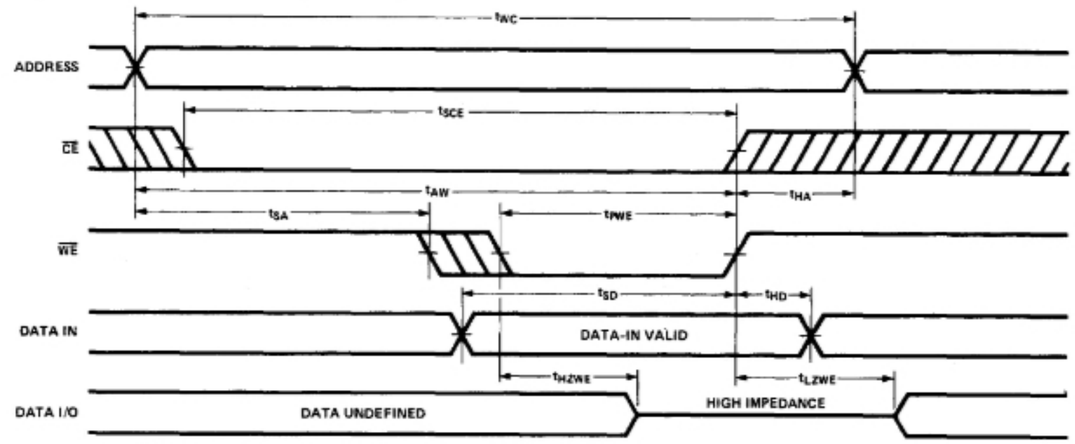


Switching Waveforms (Continued)

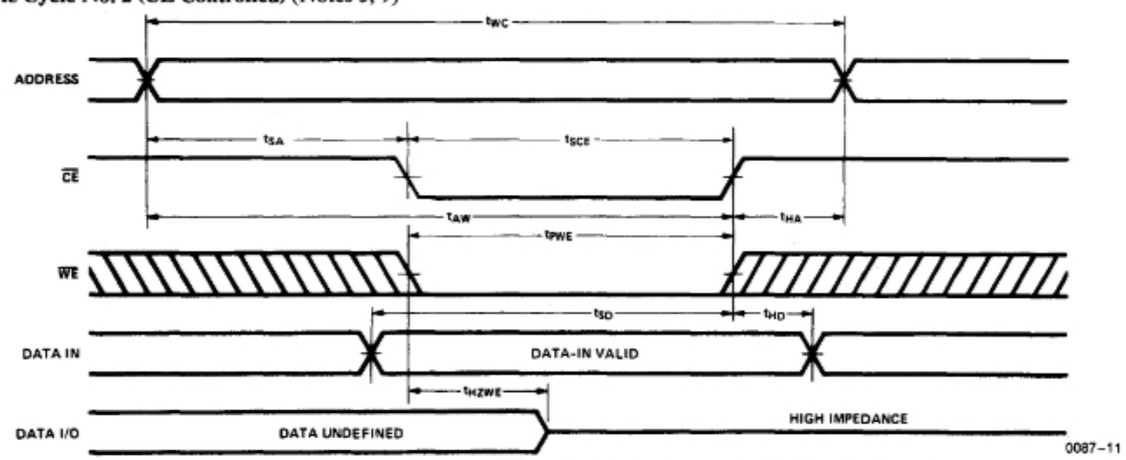
Read Cycle No. 2 (Notes 10, 12)



Write Cycle No. 1 (WE Controlled) (Notes 5, 9)



Write Cycle No. 2 (CE Controlled) (Notes 5, 9)

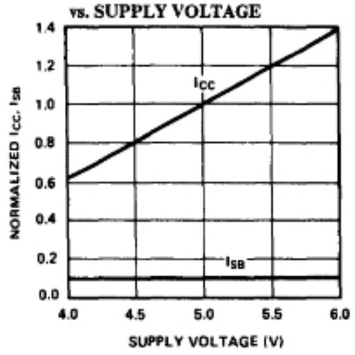


Note: If CE goes HIGH simultaneously with WE HIGH, the output remains in a high impedance state.

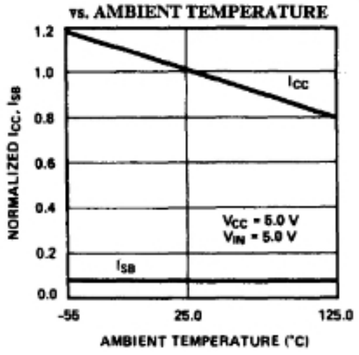
2

Typical DC and AC Characteristics

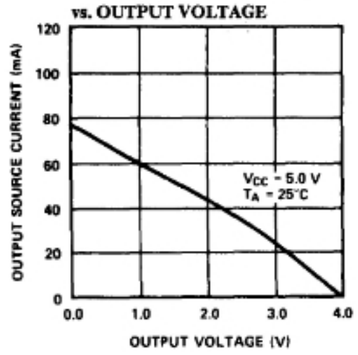
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



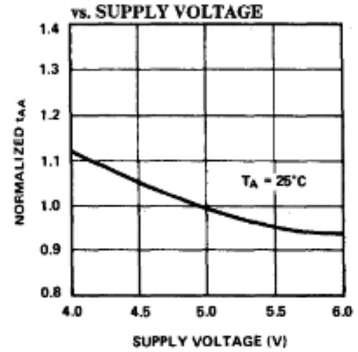
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



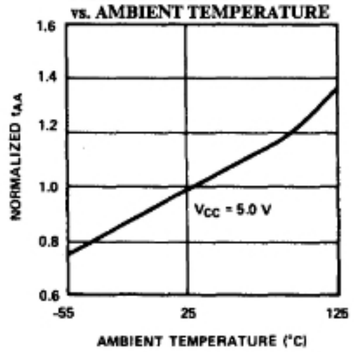
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



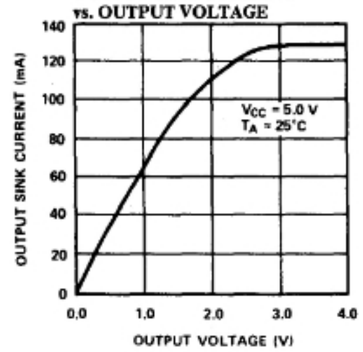
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



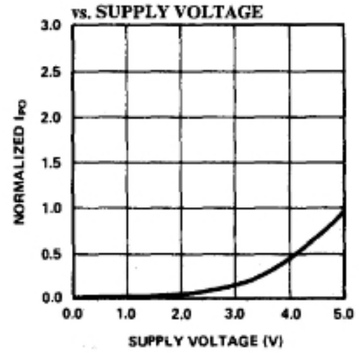
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



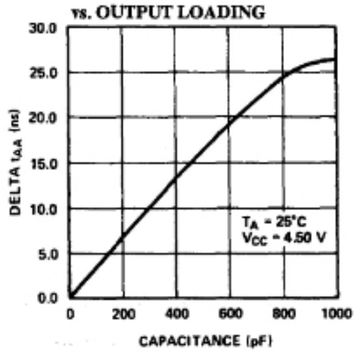
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



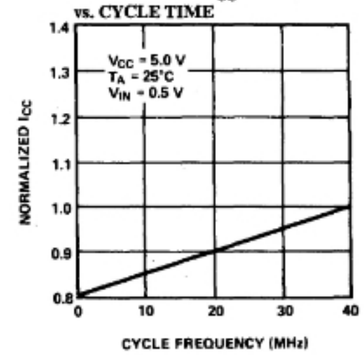
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED ICC vs. CYCLE TIME



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Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY6116-35PC CY6116-35DC CY6116-35LC	P11 D12 L64	Commercial
	CY6116-35DMB CY6116-35LMB	D12 L64	Military
45	CY6116-45PC CY6116-45DC CY6116-45LC	P11 D12 L64	Commercial
	CY6116-45DMB CY6116-45LMB	D12 L64	Military
55	CY6116-55PC CY6116-55DC CY6116-55LC	P11 D12 L64	Commercial
	CY6116-55DMB CY6116-55LMB	D12 L64	Military

Address Designators

Address Name	Address Function	Pin Number
A_0	Y_3	8
A_1	Y_2	7
A_2	Y_1	6
A_3	Y_0	5
A_4	X_2	4
A_5	X_4	3
A_6	X_3	2
A_7	X_0	1
A_8	X_5	23
A_9	X_6	22
A_{10}	X_1	19

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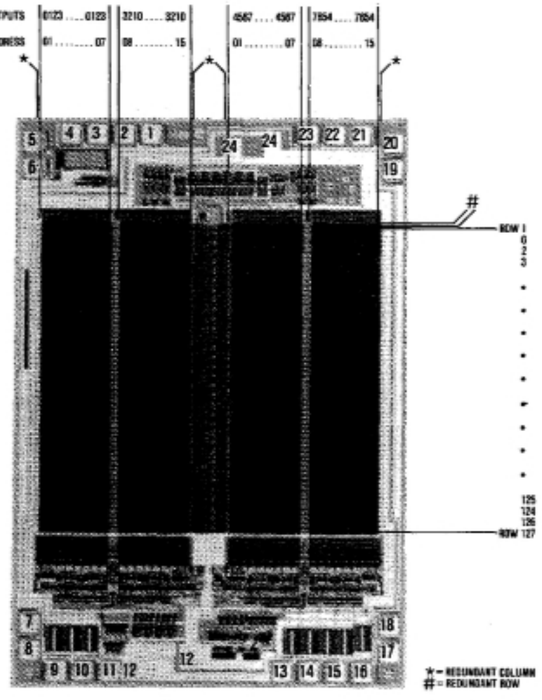
Bit Map



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MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}	1,2,3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7,8,9,10,11
t_{AA}	7,8,9,10,11
t_{OHA}	7,8,9,10,11
t_{ACE}	7,8,9,10,11
t_{DOE}	7,8,9,10,11
WRITE CYCLE	
t_{WC}	7,8,9,10,11
t_{SCE}	7,8,9,10,11
t_{AW}	7,8,9,10,11
t_{HA}	7,8,9,10,11
t_{SA}	7,8,9,10,11
t_{PWE}	7,8,9,10,11
t_{SD}	7,8,9,10,11
t_{HD}	7,8,9,10,11

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