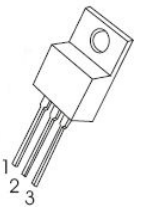
TIP120,121,122 Darlington TRANSISTOR (NPN)

TIP125,126,127 Darlington TRANSISTOR (PNP)

TO-220



1.BASE

2.COLLECTOR

3.EMITTER

FEATURES

Medium Power Complementary silicon transistors

MAXIMUM RATINGS (T_A=25℃ unless otherwise noted)

Symbol	Parameter	TIP120 TIP125	TIP121 TIP126	TIP122 TIP127	Units
V_{CBO}	Collector-Base Voltage	60	80	100	V
V_{CEO}	Collector-Emitter Voltage	60	80	100	V
V_{EBO}	Emitter-Base Voltage	5			V
I_C	Collector Current -Continuous	5			A
P_C	Collector Power Dissipation	2			W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	62.5			℃/W
$R_{\theta Jc}$	Thermal Resistance Junction to Case	1.92			℃/W
T_J	Junction Temperature	150			℃
T_{stg}	Storage Temperature	-55to+150			℃

ELECTRICAL CHARACTERISTICS (Tamb=25℃ unless otherwise specified)

Parameter		Symbol	Test conditions	MIN	MAX	UNIT
Collector-base breakdown voltage	**TIP120,TIP125** **TIP121,TIP126** **TIP122,TIP127**	$V(BR)_{CBO}$	I_C= 1mA,I_E=0	60 80 100		V
Collector-emitter breakdown voltage	**TIP120,TIP125** **TIP121,TIP126** **TIP122,TIP127**	$V_{CEO}(SUS)$	I_C= 30mA,I_B=0	60 80 100		V
Collector cut-off current	**TIP120,TIP125** **TIP121,TIP126** **TIP122,TIP127**	I_{CBO}	V_{CB}= 60 V, I_E=0 V_{CB}= 80 V, I_E=0 V_{CB}= 100V, I_E=0		0.2	mA
Collector cut-off current	**TIP120,TIP125** **TIP121,TIP126** **TIP122,TIP127**	I_{CEO}	V_{CE}=30 V, I_B=0 V_{CE}=40 V, I_B=0 V_{CE}=50 V, I_B=0		0.5	mA
Emitter cut-off current		I_{EBO}	V_{EB}=5 V, I_C=0		2	mA
DC current gain		$h_{FE(1)}$	V_{CE}= 3V, I_C=0.5A	1000		
		$h_{FE(2)}$	V_{CE}= 3V, I_C=3 A	1000		
Collector-emitter saturation voltage		V_{CE}(sat)	I_C=3A,I_B=12mA I_C=5 A,I_B=20mA		2 4	V
Base-emitter voltage		V_{BE}	V_{CE}=3V, I_C=3 A		2.5	V
Output Capacitance	**TIP125,TIP126,TIP127** **TIP120,TIP121,TIP122**	Cob	V_{CB}=10V, I_E=0,f=0.1MHz		300 200	pF

Typical Characteristics

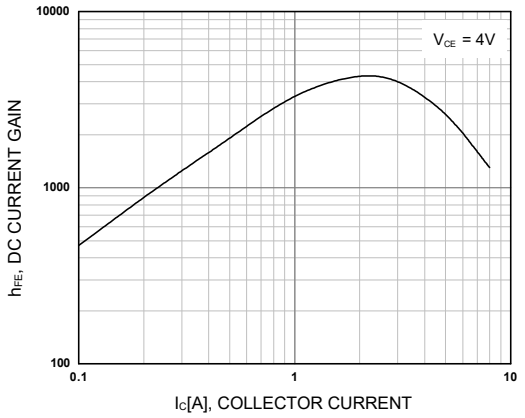


Figure 1. DC current Gain

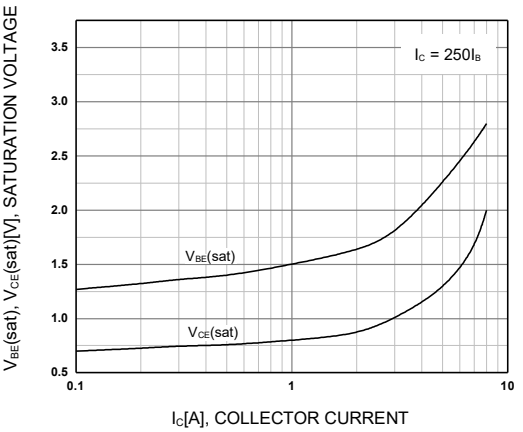


Figure 2. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

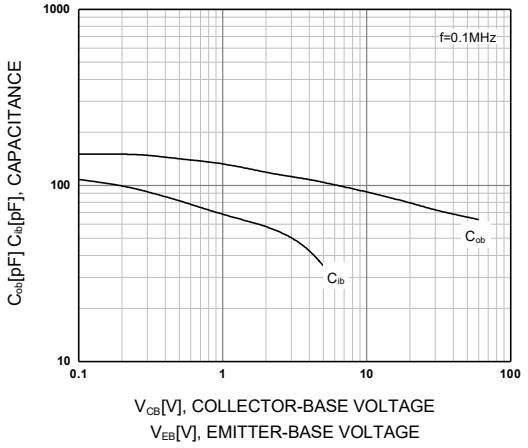


Figure 3. Output and Input Capacitance vs. Reverse Voltage

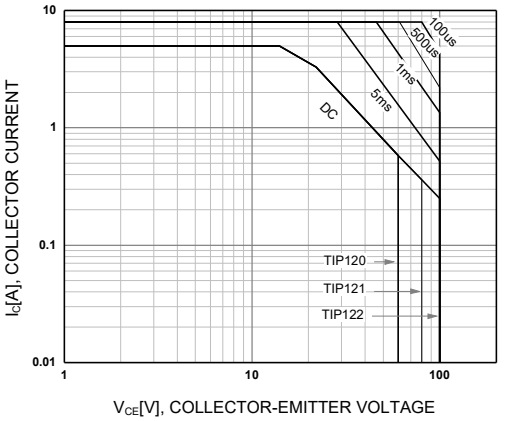


Figure 4. Safe Operating Area

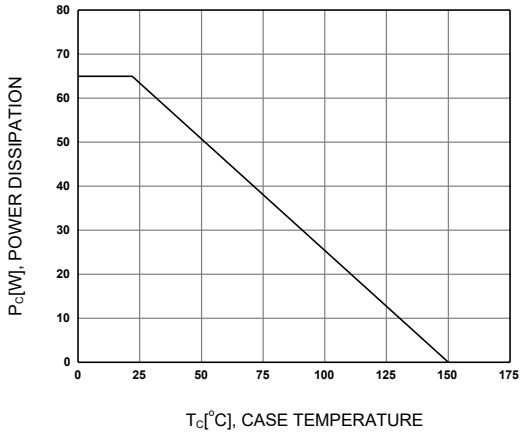


Figure 5. Power Derating